Refine Search

Search Results -

Terms	Documents
(transmit$4 or send$3) same receiv$3 same (path or bus or cable) same (bridge near20 configur$3 near20 bus)	47

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L2

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Wednesday, March 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=OR		
L2	(transmit$4 or send$3) same receiv$3 same (path or bus or cable) same (bridge near20 configur$3 near20 bus)	47	L2
L1	(transmit$4 or send$3) same receiv$3 same (path or bus or cable) same bridge	1734	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Terms	Documents
L2	0

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, March 24, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=USPT; PLUR=YES; OP=OR			
L2	(transmit$4 or send$3) same receiv$3 same (path or bus or cable) same (bridge near20 configur$3 near20 bus)	47	L2
L1	(transmit$4 or send$3) same receiv$3 same (path or bus or cable) same bridge	1734	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(370/276 |370/386 |370/401 |370/402 |370/423 |370/912 |709/230 |709/250 |709/253 |710/52 |710/62 |710/36 |710/307 |710/2 |710/33 |710/300 |710/306 |710/313).ccls.	6644

Database:
US Pre-Grant Publication Full-Text Database
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US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
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IBM Technical Disclosure Bulletins

Search: L1

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Thursday, March 25, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count
	DB=USPT; PLUR=YES; OP=OR	
L1	710/52,62,36,307,2,33,300,306,313;709/230,250,253;370/276,386,401,402,423,912.ccls.	6644

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L2	22

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text Clear Interrupt

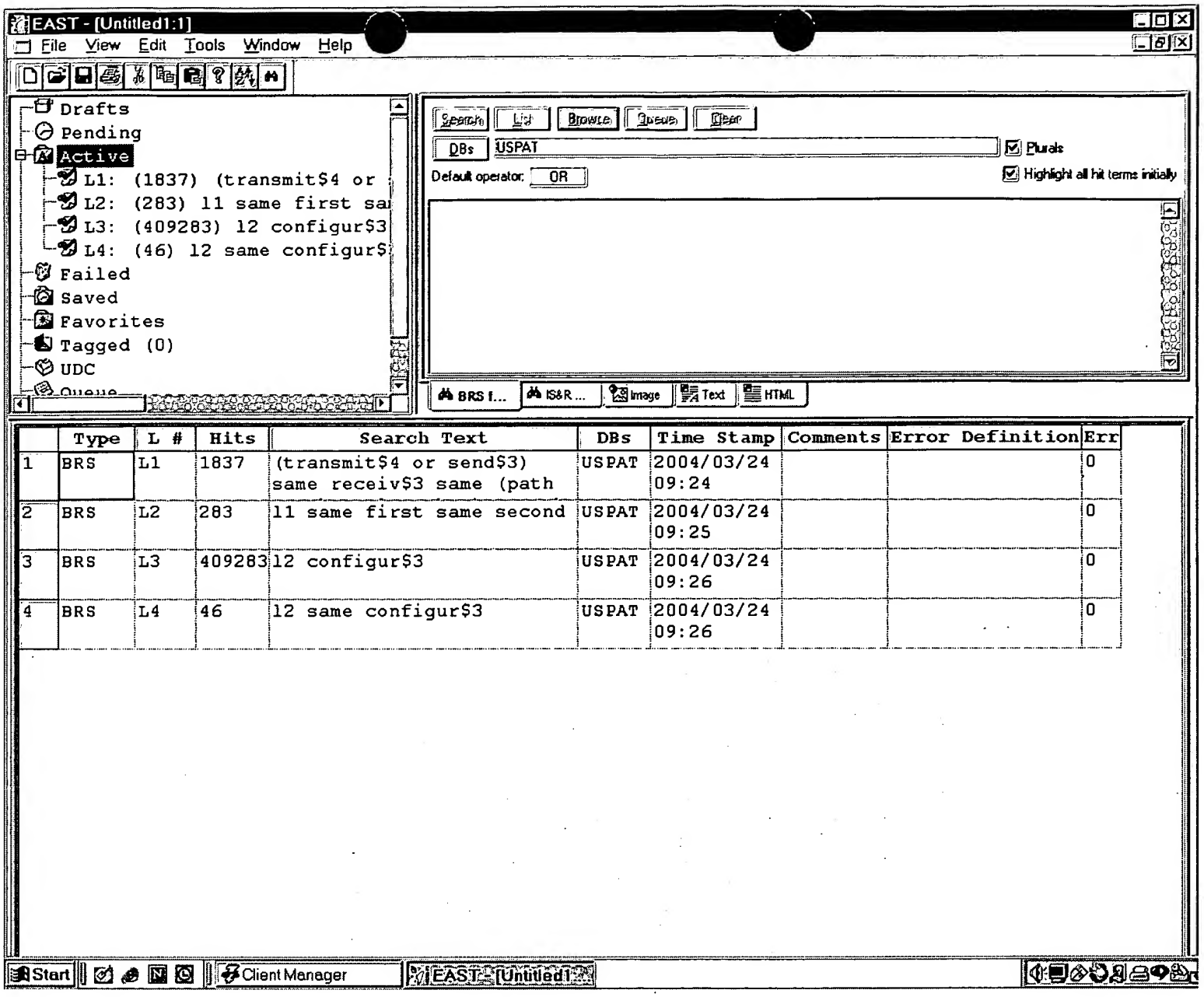
Search History

DATE: Thursday, March 25, 2004 Printable Copy Create Case

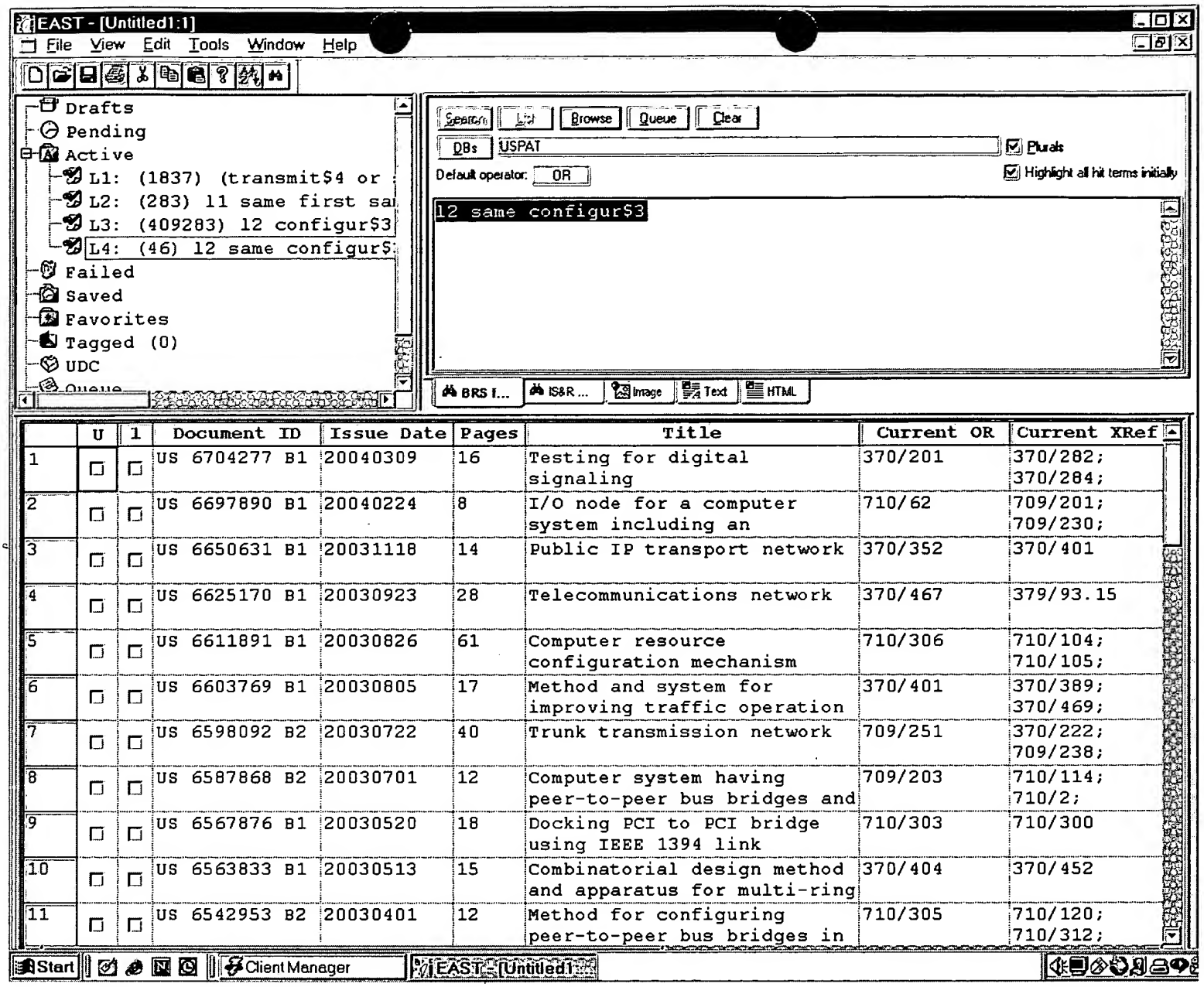
Set Name side by side	Query	Hit Count
	DB=USPT; PLUR=YES; OP=OR	
L3	l1 and L2	22
L2	(transmit$4 or send$3) same receiv$3 same (path or bus or cable) same (bridge near20 configur$3 near20 bus)	47
L1	710/52,62,36,307,2,33,300,306,313;709/230,250,253;370/276,386,401,402,423,912.ccls.	6644

END OF SEARCH HISTORY

h e b b cg b e e ch



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	1837	(transmit$4 or send$3) same receiv$3 same (path	USPAT	2004/03/24 09:24			0
2	BRS	L2	283	l1 same first same second	USPAT	2004/03/24 09:25			0
3	BRS	L3	409283	l2 configur$3	USPAT	2004/03/24 09:26			0
4	BRS	L4	46	l2 same configur$3	USPAT	2004/03/24 09:26			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6704277 B1	20040309	16	Testing for digital signaling	370/201	370/282; 370/284;
2	☐	☐	US 6697890 B1	20040224	8	I/O node for a computer system including an	710/62	709/201; 709/230;
3	☐	☐	US 6650631 B1	20031118	14	Public IP transport network	370/352	370/401
4	☐	☐	US 6625170 B1	20030923	28	Telecommunications network	370/467	379/93.15
5	☐	☐	US 6611891 B1	20030826	61	Computer resource configuration mechanism	710/306	710/104; 710/105;
6	☐	☐	US 6603769 B1	20030805	17	Method and system for improving traffic operation	370/401	370/389; 370/469;
7	☐	☐	US 6598092 B2	20030722	40	Trunk transmission network	709/251	370/222; 709/238;
8	☐	☐	US 6587868 B2	20030701	12	Computer system having peer-to-peer bus bridges and	709/203	710/114; 710/2;
9	☐	☐	US 6567876 B1	20030520	18	Docking PCI to PCI bridge using IEEE 1394 link	710/303	710/300
10	☐	☐	US 6563833 B1	20030513	15	Combinatorial design method and apparatus for multi-ring	370/404	370/452
11	☐	☐	US 6542953 B2	20030401	12	Method for configuring peer-to-peer bus bridges in	710/305	710/120; 710/312;

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(transmit* or send*) and receiv*<and>bridge and bu Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **On the wavelength assignment problem of multi-channel photonic c bus networks**
Nen-Fu Huang; Shiann-Tsong Sheu;
Global Telecommunications Conference, 1994. GLOBECOM '94. 'Communicati The Global Bridge'., IEEE , Volume: 3 , 28 Nov.-2 Dec. 1994
Pages:1925 - 1929 vol.3

[Abstract] [PDF Full-Text (552 KB)] **IEEE CNF**

---

2 **The STAR DAQ receiver board**
LeVine, M.J.; Ljubicic, A., Jr.; Schulz, M.W.; Scheetz, R.; Consiglio, C.; Padra D.; Zhao, Y.;
Nuclear Science, IEEE Transactions on , Volume: 47 , Issue: 2 , April 2000
Pages:127 - 131

[Abstract] [PDF Full-Text (288 KB)] **IEEE JNL**

---

3 **An innovative technique for packaging power electronic building blc using metal posts interconnected parallel plate structures**
Haque, S.; Kun Xing; Ray-Lee Lin; Suchicital, C.T.A.; Guo-Quan Lu; Nelson, I Borojevic, D.; Lee, F.C.;
Advanced Packaging, IEEE Transactions on [see also Components, Packaging Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on] , Volume: 22 , Issue: 2 , May 1999
Pages:136 - 144

[Abstract] [PDF Full-Text (508 KB)] **IEEE JNL**

---

4 **The STAR DAQ receiver board**
LeVine, M.J.; Ljubicic, A., Jr.; Schulz, M.W.; Scheetz, R.; Consiglio, C.; Padra.

D.; Zhao, Y.;
Real Time Conference, 1999. Santa Fe 1999. 11th IEEE NPSS , 14-18 June 1
Pages:99 - 103

[Abstract] [PDF Full-Text (348 KB)] **IEEE CNF**

---

5 **An innovative technique for packaging power electronic building bl using metal posts interconnected parallel plate structures**
Haque, S.; Kun Xing; Ray-Lee Lin; Suchicital, C.; Lu, G.-Q.; Nelson, D.J.; Borojevic, D.; Lee, F.C.;
Electronic Components and Technology Conference, 1998. 48th IEEE , 25-28 1998
Pages:922 - 929

[Abstract] [PDF Full-Text (1048 KB)] **IEEE CNF**

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On the wavelength assignment problem of multi-channel photonic dual bus networks

Nen-Fu Huang Shiann-Tsong Sheu
Dept. of Comput. Sci., Nat. Tsing Hua Univ., Hsinchu, Taiwan;

This paper appears in: **Global Telecommunications Conference, 1994. GLOBECOM '94. 'Communications: The Global Bridge'., IEEE**

Meeting Date: 11/28/1994 - 12/02/1994
Publication Date: 28 Nov.-2 Dec. 1994
Location: San Francisco, CA USA
On page(s): 1925 - 1929 vol.3
Volume: 3
Reference Cited: 12
Inspec Accession Number: 5086339

Abstract:
In a multi-channel photonic dual **bus** network, each unidirectional **bus** contains a control channel and several data channels (wavelengths), and each station has n tunable **transmitters** and m tunable **receivers**. Given a set of serving traffic and a set of new traffic requests, the wavelength assignment problem ((n,m)-WAP) is to assign the transmission wavelengths and **receiving** wavelengths of each station so that all the traffic requests can be served simultaneously and the number of assigned wavelengths is

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minimized. In this paper, we prove that the (n,m)-WAP is NP-complete by showing that the simplified version of the (n,m)-WAP (SWAP, or (1,1)-WAP), in which each station has only one tunable **transmitter** and one tunable **receiver**, is NP-complete. An efficient distributed wavelength assignment algorithm (DWAA) is proposed for the (1,m)-WAP. The throughput and delay characteristics of the DWAA is evaluated by simulation. Simulation results show that for a limited number of available wavelengths, the solutions obtained by the DWAA is attractive in terms of throughput, access delay, as well as fairness, under general traffic demands

Index Terms:

NP-complete computational complexity control channel data channels delay characteristics distributed wavelength assignment algorithm multi-channel photonic dual **bus** networks optical fibre networks protocols **receiving** wavelengths simulation system buses telecommunication traffic throughput characteristics traffic requests transmission wavelengths tunable **receivers** tunable **transmitters** unidirectional **bus** wavelength assignment problem wavelength division multiplexing NP-complete computational complexity control channel data channels delay characteristics distributed wavelength assignment algorithm multi-channel photonic dual **bus** networks optical fibre networks protocols **receiving** wavelengths simulation system buses telecommunication traffic throughput characteristics traffic requests transmission wavelengths tunable **receivers** tunable **transmitters** unidirectional **bus** wavelength assignment problem wavelength division multiplexing

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The STAR DAQ receiver board

LeVine, M.J. Ljubicic, A., Jr. Schulz, M.W. Scheetz, R. Consiglio, C. Padrazo, D. Zhao, Y.
Brookhaven Nat. Lab., Upton, NY, USA ;
This paper appears in: **Nuclear Science, IEEE Transactions on**

Meeting Date: 06/14/1999 - 06/18/1999
Publication Date: April 2000
Location: Sante Fe, NM USA
On page(s): 127 - 131
Volume: 47 , Issue: 2
ISSN: 0018-9499
Reference Cited: 5
CODEN: IETNAE
Inspec Accession Number: 6632220

Abstract:
Data digitized on the STAR TPC detector are **transmitted** via 1.5 Gbit/sec optical fiber to the DAQ **receiver** boards (RB) located in Sector VME crates. The RE contains the optical **receiver**, Glink decoder, high speed **bus** to deliver data to three Mezzanines, which perform the processing. The RE back end provides an interface between VME64 and PCI, serving as interconnect between all of the Mezzanines, the VME **bus**, and resources local to the **receiver** board. Each Mezzanine hosts an Intel I960HD superscalar RISC CPU,

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which performs 2-dimensional cluster-finding and data formatting. Dual-ported VRAM provide storage for 12 TPC events. Incoming data are processed in real time by a bank of ASICs which perform pedestal subtraction, 10-bit to 8-bit compression via table lookup, and compilation of a sequence pointer bank for use by the CPU during cluster-finding. Communication among the I960s and the master CPU in the VME crate takes place through mailboxes and doorbells implemented in the I960-PCI **bridge** chips

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Index Terms:

data acquisition nuclear electronics optical fibre communication system buses time projection chambers DAQ **receiver** boards Glink decoder Intel I960HD superscalar RISC CPU Mezzanines STAR DAQ **receiver** board STAR time projection chamber VME crates data formatting optical **receiver** pedestal subtraction sequence pointer bank table lookup two-dimensional cluster-finding

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L2: Entry 1 of 47 File: USPT Feb 24, 2004

US-PAT-NO: 6697890
DOCUMENT-IDENTIFIER: US 6697890 B1

TITLE: I/O node for a computer system including an integrated I/O interface

DATE-ISSUED: February 24, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gulick; Dale E.	Austin	TX		
Hewitt; Larry D.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 10/ 034878 [PALM]
DATE FILED: December 27, 2001

INT-CL: [07] G06 F 13/12

US-CL-ISSUED: 710/62; 710/33, 710/36, 710/106, 709/201, 709/230
US-CL-CURRENT: 710/62; 709/201, 709/230, 710/106, 710/33, 710/36

FIELD-OF-SEARCH: 710/1, 710/15, 710/17, 710/18, 710/29, 710/31, 710/33, 710/36, 710/38, 710/41, 710/62, 710/64, 710/72, 710/105, 710/106, 712/29, 712/225, 709/201, 709/230

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5432907	July 1995	Picazo, Jr. et al.	395/200
☐	5490168	February 1996	Phillips et al.	375/224
☐	5812930	September 1998	Zavrel	455/5.1
☐	5859848	January 1999	Miura et al.	370/395
☐	6278532	August 2001	Heimendinger et al.	
☐	6282714	August 2001	Ghori et al.	725/81
	6359907	March 2002	Wolters et al.	370/485

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☐				
☐	6414525	July 2002	Urakawa	
☐	6532283	March 2003	Ingram	379/130

OTHER PUBLICATIONS

U.S. patent application Ser. No. 09/978,349, filed Oct. 15, 2001.
U.S. patent application Ser. No. 10/093,146, filed Mar. 7, 2002.

ART-UNIT: 2182

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Mai; Rijue

ATTY-AGENT-FIRM: Meyertons Hood Kivlin Kowert & Goetzel, P.C. Kivlin; B. Noel

ABSTRACT:

An I/O node for a computer system including an integrated I/O interface. An input/output node for a computer system that is implemented upon an integrated circuit includes a first transceiver unit, a second transceiver unit, a packet tunnel, a bridge unit and an I/O interface unit. The first transceiver unit may receive and transmit packet transactions on a first link of a packet bus. The second transceiver unit may receive and transmit packet transactions on a second link of the packet bus. The packet tunnel may convey selected packet transactions between the first and second transceiver units. The bridge unit may receive particular packet transactions from the first transceiver may transmit transactions corresponding to the particular packet transactions upon a peripheral bus. The I/O interface unit may receive additional packet transactions from the first transceiver unit and may transmit transactions corresponding to the additional packet transactions upon an I/O link.

20 Claims, 2 Drawing figures

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L3: Entry 19 of 22 File: USPT Oct 20, 1998

US-PAT-NO: 5826048
DOCUMENT-IDENTIFIER: US 5826048 A

TITLE: PCI bus with reduced number of signals

DATE-ISSUED: October 20, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dempsey; Morgan James	Phoenix	AZ		
Jayavant; Rajeev	Phoenix	AZ		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
VLSI Technology, Inc.	San Jose	CA			02

APPL-NO: 08/ 790303 [PALM]
DATE FILED: January 31, 1997

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/309; 395/308
US-CL-CURRENT: 710/306

FIELD-OF-SEARCH: 395/306, 395/308, 395/309, 395/285

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5455915	October 1995	Coke	395/293
☐	5644734	July 1997	Houg	395/309
☐	5740385	April 1998	Hayek et al.	395/308

ART-UNIT: 271

PRIMARY-EXAMINER: Auve; Glenn A.

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ATTY-AGENT-FIRM: Hickman & Martine, LLP

ABSTRACT:

A Mini-PCI (MPCI) interface, and associated circuits and methods are provided for connecting a Peripheral Component Interconnect (PCI) device to one or more external devices. The MPCI interface, circuits and methods provide for a substantial if not full implementation of a PCI Local Bus without requiring the standard number of pins, traces, or signals. The MPCI interface includes a PCI/MPCI bridge connected between a PCI bus and to up to eight external devices in the form of MPCI devices and linear memory devices. The PCI/MPCI bridge is capable of receiving an incoming PCI transaction and multiplexing some of its signals together to create a corresponding incoming MPCI transaction. This incoming MPCI transaction may then be passed over an MPCI bus, having fewer lines and optimally operating at a higher frequency, the external devices. The process is reversed for outgoing transactions, i.e., the MPCI transactions are de-multiplexed to create PCI transactions. Additionally, the MPCI interface may also be configured to provide for direct access to linearly addressed memory devices without adding a PCI interface to the external interface. The invention may be implemented through integrated circuitry and/or computer implemented instructions, and may be included within a personal computer.

22 Claims, 12 Drawing figures

First Hit Fwd Refs

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L3: Entry 21 of 22 File: USPT Jun 23, 1998

US-PAT-NO: 5771360
DOCUMENT-IDENTIFIER: US 5771360 A

TITLE: PCI bus to target integrated circuit interconnect mechanism allowing multiple bus masters and two different protocols on the same bus

DATE-ISSUED: June 23, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gulick; Dale E.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 08/ 731829 [PALM]
DATE FILED: October 21, 1996

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/308; 395/285, 395/281, 395/527
US-CL-CURRENT: 710/307; 703/27, 710/105

FIELD-OF-SEARCH: 395/308, 395/285, 395/306, 395/281, 395/309, 395/527, 395/291, 395/500, 370/285, 327/423

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5526349	June 1996	Diaz et al.	370/58.1
☐	5664124	September 1997	Katz et al.	395/309
☐	5682484	October 1997	Lambrecht	395/308

OTHER PUBLICATIONS

PCI Local Bus Multimedia Design Guide, Revision 1.0, Mar. 28, 1994, pp. 1-40.
Peripheral Components, Intel, Jan. 1995, pp. ix, 1-1 through 1-72.

h e b b g e e e f c e e ge

ART-UNIT: 271

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Seto; Jeffrey K.

ATTY-AGENT-FIRM: Conley, Rose & Tayon Kivlin; B. Noel

ABSTRACT:

A computer system comprising a first expansion bus which operates according to a first transfer protocol and is adapted to couple to one or more peripheral devices. A central processing unit and a bus bridge are operatively coupled to the first expansion bus. A second bus including a second transfer protocol is coupled to the bus bridge. At least one peripheral device of a first type compatible with the second transfer protocol is coupled to the second bus. At least one peripheral device of a second type coupled to the second bus, wherein the at least one peripheral device of the second type is compatible with a third transfer protocol of a peripheral bus standard, the third transfer protocol of the peripheral bus standard being different from the second transfer protocol of the second bus. The bus bridge is operable to convert signals between the first expansion bus and the second bus, and is operable to implement the second transfer protocol on the second bus. The bus bridge is also operable to implement the third transfer protocol of the peripheral bus standard on the second bus. The bus bridge is configured to communicate with the at least one peripheral device of the first type using the second transfer protocol of the second bus, and is configured to communicate with the at least one peripheral device of the second type using the third transfer protocol of the peripheral bus standard.

26 Claims, 34 Drawing figures

First Hit Fwd Refs

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L2: Entry 1 of 47 File: USPT Feb 24, 2004

DOCUMENT-IDENTIFIER: US 6697890 B1
TITLE: I/O node for a computer system including an integrated I/O interface

Brief Summary Text (14):
The first transceiver unit may be configured to receive and transmit packet transactions on a first link of a packet bus. The second transceiver unit may be coupled to receive and transmit packet transactions on a second link of the packet bus. The packet tunnel is coupled to convey selected packet transactions between the first transceiver unit and the second transceiver unit. The bridge unit is coupled to receive particular packet transactions from the first transceiver and may be configured to transmit transactions corresponding to the particular packet transactions upon a peripheral bus, such as for example, a PCI-X bus. The I/O interface unit is coupled to receive additional packet transactions from the first transceiver and may be configured to transmit transactions corresponding to the additional packet transactions upon an I/O link, such as an Ethernet link, for example.

Brief Summary Text (17):
In another implementation, the bridge unit may be further configured to receive peripheral transactions from the peripheral bus and to transmit transactions corresponding to the peripheral transactions to the first transceiver unit.

CLAIMS:

1. An input/output node for a computer system, said input/output node comprising: a first transceiver unit implemented on an integrated circuit chip, wherein said first transceiver unit is configured to receive and transmit packet transactions on a first link of a packet bus; a second transceiver unit implemented on said integrated circuit chip, wherein said second transceiver unit is coupled to receive and transmit packet transactions on a second link of said packet bus; a packet tunnel implemented on said integrated circuit chip, wherein said packet tunnel is coupled to convey selected packet transactions between said first transceiver unit and said second transceiver unit; a bridge unit implemented on said integrated circuit chip, wherein said bridge unit is coupled to receive particular packet transactions from said first transceiver and is configured to transmit transactions corresponding to said particular packet transactions upon a peripheral bus; and an I/O interface unit implemented on said integrated circuit chip, wherein said I/O interface unit is coupled to receive additional packet transactions from said first transceiver and is configured to transmit transactions corresponding to said additional packet transactions upon an I/O link.

4. The input/output node as recited in claim 3, wherein said bridge unit is further configured to receive peripheral transactions from said peripheral bus and to transmit transactions corresponding to said peripheral transactions to said first transceiver unit.

11. A computer system comprising: a processor; a first link of a packet bus coupled to said processor; an input/output node coupled to said first link, said input/output node including: a first transceiver unit implemented on an integrated circuit chip, wherein said first transceiver unit is configured to receive and

transmit packet transactions on said first link of a packet bus; a second transceiver unit implemented on said integrated circuit chip, wherein said second transceiver unit is coupled to receive and transmit packet transactions on a second link of said packet bus; a packet tunnel implemented on said integrated circuit chip, wherein said packet tunnel is coupled to convey selected packet transactions between said first transceiver unit and said second transceiver unit; a bridge unit implemented on said integrated circuit chip, wherein said bridge unit is coupled to receive particular packet transactions from said first transceiver and is configured to transmit transactions corresponding to said particular packet transactions upon a peripheral bus; and an I/O interface unit implemented on said integrated circuit chip, wherein said I/O interface unit is coupled to receive additional packet transactions from said first transceiver and is configured to transmit transactions corresponding to said additional packet transactions upon an I/O link.

14. The computer system as recited in claim 13, wherein said bridge unit is further configured to receive peripheral transactions from said peripheral bus and to transmit transactions corresponding to said peripheral transactions to said first transceiver unit.

L2: Entry 45 of 47 File: USPT Jun 23, 1998

DOCUMENT-IDENTIFIER: US 5771360 A
TITLE: PCI bus to target integrated circuit interconnect mechanism allowing multiple bus masters and two different protocols on the same bus

Brief Summary Text (15):
A variety of transfer methods according to the present invention are contemplated. A method of transferring data in a computer system using inherent flow control according to one embodiment of the present invention devices comprises activating a source port in a bus bridge to configure the source port in the bus bridge for a transfer. Next, an address identifying a destination port on one of a plurality of peripheral devices is received from the first bus and stored in a register in the source port. Once the address has been received, data that is to be transmitted to a peripheral device is received from the first bus, and stored in a buffer in the bus bridge. The data are transmitted to the peripheral device as one or more address/data pairs, each of which includes the address and the data received from the first bus.

Brief Summary Text (16):
A method of communicating in a computer system employing external inherent flow control comprises first activating a source port in a bus bridge to configure the source port a transfer. Next, an address identifying a destination port in a peripheral device is received from a first bus and is stored in a register of the source port. Data from the first bus that is to be transferred to a destination port of a peripheral device is stored in a buffer in the source port. The data are transmitted as one or more address/data pairs to the destination port. If the buffer in the bus bridge is substantially empty, and the target peripheral requires more data, it transmits a flow control command. A receive port in the bus bridge receives the flow control command, and the bus bridge retrieves data from memory in the computer system in response to the request. The requested data are transmitted as one or more address/data pairs to the destination port of the target peripheral device.

Brief Summary Text (18):
The first method generates interrupts to a peripheral device. Initially, a source port in the bus bridge is configured for a transfer. Next, an encoded interrupt vector is received from the first bus and is stored in a register of the source port. The encoded interrupt vector is indicative of one or more interrupt requests directed to a target peripheral device. An address/data pair containing the encoded interrupt vector is transmitted to a destination port of the peripheral device. Once received, the encoded interrupt vector is stored in a register of the destination port. Once the encoded interrupt vector is read, the peripheral device executes the appropriate interrupt routine.

Brief Summary Text (19):
The second method generates interrupts at a CPU. Initially, a destination port in the bus bridge is configured for a transfer. A digital signal processor in a source peripheral device next activates a source port in the source peripheral device. The source peripheral device transmits a command message as address/data pairs to the bus bridge responsive to said digital signal processor activating said source port. The bus bridge receiving the command message and sets a bit in a register

responsive to receiving the command message. Finally, an interrupt is generated to the CPU in response to the setting of the bit.

Brief Summary Text (21):
Yet another embodiment of the present invention provides a method for moving large blocks of data to and from memory. For example, a method for transferring data from a memory starts by activating a source port in a bus bridge to configure the source port for a transfer. Next, memory address and transfer size information is received from a device such as a main memory on a first bus, and is stored in a register of the source port. The memory address and transfer size information is indicative of a location and amount of data to be transmitted to a target peripheral device. A command message is then transmitted to a destination port of the target peripheral device. The command includes an address of the destination port and memory address and transfer size information. The target executes an interrupt in response to receiving the command, and activates a data port in response to the interrupt. The source port receives data from the first bus into a buffer and transfers it as one or more address/data pairs to a data port on the peripheral device. The address/data pairs each include an address of the data port received from the first bus.

Detailed Description Text (10):
Turning now to FIG. 2, the MoTel Bus system is shown in greater detail. MoTel Bus bridge 68, MoTel Bus devices 72a through 72c employing the MoTel bus transfer protocol, and a non-MoTel Bus device 74 employing a non-MoTel bus transfer protocol, such as an ISA bus transfer protocol, and logic circuit or address latch 76 are coupled to MoTel Bus 70. In a preferred embodiment, host PC 55 includes a PCI interface 100 coupled to a PCI bus 60, which in turn is coupled to a PCI interface 102 on MoTel Bus bridge 68. MoTel Bus bridge 68 further includes a plurality of bus bridge ports 106. The bus bridge ports comprise transmit and receive ports, a predetermined number of which are configured to be selectively activated at a given time.

CLAIMS:

7. The computer system of claim 1, wherein the at least one peripheral device of the first type comprises at least one destination port for receiving data transmissions from the bus bridge on the second bus using the second transfer protocol; and

wherein the bus bridge comprises:

a transceiver configured to interface data transmissions on the second bus using the second transfer protocol; and

at least one transmit port operatively coupled to the transceiver, the at least one transmit port comprising:

a data buffer for receiving data to be transmitted over the second bus; and

a transmit port state machine coupled to the data buffer and configured to identify a destination port address of the at least one destination port on the at least one peripheral device of the first type for receiving data transmissions from the bus bridge on the second bus using the second transfer protocol.

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L2: Entry 45 of 47 File: USPT Jun 23, 1998

US-PAT-NO: 5771360
DOCUMENT-IDENTIFIER: US 5771360 A

TITLE: PCI bus to target integrated circuit interconnect mechanism allowing multiple bus masters and two different protocols on the same bus

DATE-ISSUED: June 23, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gulick; Dale E.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 08/ 731829 [PALM]
DATE FILED: October 21, 1996

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/308; 395/285, 395/281, 395/527
US-CL-CURRENT: 710/307; 703/27, 710/105

FIELD-OF-SEARCH: 395/308, 395/285, 395/306, 395/281, 395/309, 395/527, 395/291, 395/500, 370/285, 327/423

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5526349	June 1996	Diaz et al.	370/58.1
☐	5664124	September 1997	Katz et al.	395/309
☐	5682484	October 1997	Lambrecht	395/308

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Peripheral Components, Intel, Jan. 1995, pp. ix, 1-1 through 1-72.

h e b b g e e e f c e c e ge

ART-UNIT: 271

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Seto; Jeffrey K.

ATTY-AGENT-FIRM: Conley, Rose & Tayon Kivlin; B. Noel

ABSTRACT:

A computer system comprising a first expansion bus which operates according to a first transfer protocol and is adapted to couple to one or more peripheral devices. A central processing unit and a bus bridge are operatively coupled to the first expansion bus. A second bus including a second transfer protocol is coupled to the bus bridge. At least one peripheral device of a first type compatible with the second transfer protocol is coupled to the second bus. At least one peripheral device of a second type coupled to the second bus, wherein the at least one peripheral device of the second type is compatible with a third transfer protocol of a peripheral bus standard, the third transfer protocol of the peripheral bus standard being different from the second transfer protocol of the second bus. The bus bridge is operable to convert signals between the first expansion bus and the second bus, and is operable to implement the second transfer protocol on the second bus. The bus bridge is also operable to implement the third transfer protocol of the peripheral bus standard on the second bus. The bus bridge is configured to communicate with the at least one peripheral device of the first type using the second transfer protocol of the second bus, and is configured to communicate with the at least one peripheral device of the second type using the third transfer protocol of the peripheral bus standard.

26 Claims, 34 Drawing figures

US-PAT-NO: 6697890

DOCUMENT-IDENTIFIER: US 6697890 B1

TITLE: I/O node for a computer system including an integrated I/O interface

---------- KWIC ---------

Brief Summary Text - BSTX (14):

The first transceiver unit may be configured to receive and transmit packet transactions on a first link of a packet bus. The second transceiver unit may be coupled to receive and transmit packet transactions on a second link of the packet bus. The packet tunnel is coupled to convey selected packet transactions between the first transceiver unit and the second transceiver unit. The bridge unit is coupled to receive particular packet transactions from the first transceiver and may be configured to transmit transactions corresponding to the particular packet transactions upon a peripheral bus, such as for example, a PCI-X bus. The I/O interface unit is coupled to receive additional packet transactions from the first transceiver and may be configured to transmit transactions corresponding to the additional packet transactions upon an I/O link, such as an Ethernet link, for example.

Claims Text - CLTX (1):

1. An input/output node for a computer system, said input/output node comprising: a first transceiver unit implemented on an integrated circuit chip, wherein said first transceiver unit is configured to receive and transmit packet transactions on a first link of a packet bus; a second transceiver unit implemented on said integrated circuit chip, wherein said second transceiver unit is coupled to receive and transmit packet transactions on a second link of said packet bus; a packet tunnel implemented on said integrated circuit chip, wherein said packet tunnel is coupled to convey selected packet transactions between said first transceiver unit and said second transceiver unit; a bridge unit implemented on said integrated circuit chip, wherein said bridge unit is coupled to receive particular packet transactions from said first transceiver and is configured to transmit transactions corresponding to said particular packet transactions upon a peripheral bus; and an I/O interface unit implemented on said integrated circuit chip, wherein said I/O interface unit is

(12) **United States Patent**
Gulick et al.

(10) **Patent No.: US 6,697,890 B1**
(45) **Date of Patent: Feb. 24, 2004**

(54) **I/O NODE FOR A COMPUTER SYSTEM INCLUDING AN INTEGRATED I/O INTERFACE**

(75) Inventors: **Dale E. Gulick**, Austin, TX (US); **Larry D. Hewitt**, Austin, TX (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 235 days.

(21) Appl. No.: 10/034,878

(22) Filed: Dec. 27, 2001

(51) Int. Cl.[7] G06F 13/12

(52) U.S. Cl. 710/62; 710/33; 710/36; 710/106; 709/201; 709/230

(58) Field of Search 710/1, 15, 17, 710/18, 29, 31, 33, 36, 39, 41, 62, 64, 72, 105, 106; 712/29, 225; 709/201, 230

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U.S. patent application Ser. No. 10/093,146, filed Mar. 7, 2002.

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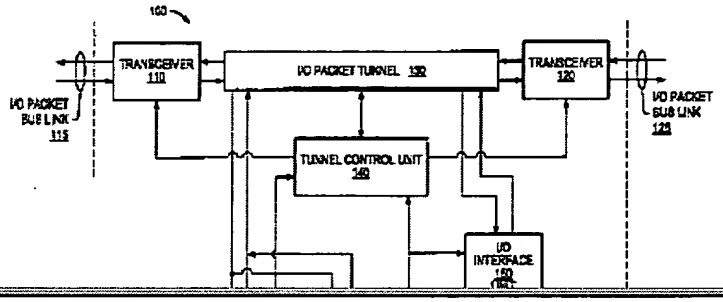
Primary Examiner—Jeffrey Gaffin
Assistant Examiner—Rijue Mai
(74) *Attorney, Agent, or Firm*—Meyertons Hood Kivlin Kowert & Goetzel, P.C.; B. Noël Kivlin

(57) **ABSTRACT**

An I/O node for a computer system including an integrated I/O interface. An input/output node for a computer system that is implemented upon an integrated circuit includes a first transceiver unit, a second transceiver unit, a packet tunnel, a bridge unit and an I/O interface unit. The first transceiver unit may receive and transmit packet transactions on a first link of a packet bus. The second transceiver unit may receive and transmit packet transactions on a second link of the packet bus. The packet tunnel may convey selected packet transactions between the first and second transceiver units. The bridge unit may receive particular packet transactions from the first transceiver may transmit transactions corresponding to the particular packet transactions upon a peripheral bus. The I/O interface unit may receive additional packet transactions from the first transceiver unit and may transmit transactions corresponding to the additional packet transactions upon an I/O link.

20 Claims, 2 Drawing Sheets



US-PAT-NO: 6567876

DOCUMENT-IDENTIFIER: US 6567876 B1

TITLE: Docking PCI to PCI bridge using IEEE 1394 link

---------- KWIC ---------

Claims Text - CLTX (23):

23. A docking bridge for interfacing a computer system and an expansion base, comprising: a first bus interface configured to transmit and receive data over a first bus and to capture the values of signals from said first bus; an encoder configured to capture sideband signals running between the computer and the expansion base and that receives the captured values from said first bus interface; a packetizer coupled to said encoder and that creates data packets containing captured signal values in said encoder; and a bus driver coupled to said packetizer and configured to transmit and receive data packets over a second bus.

US-PAT-NO: 5832245

DOCUMENT-IDENTIFIER: US 5832245 A
See image for Certificate of Correction

TITLE: Method for isochronous flow control across an inter-chip bus

---------- KWIC ---------

Abstract Text - ABTX (1):

A method for communicating data to a plurality of peripheral devices in a computer system, the computer system comprising a first bus, a bus bridge for coupling to the first bus and for interfacing to a second bus, a second bus coupled to the bus bridge, and a plurality of peripheral devices connected to the second bus. The method comprises activating a source port in the bus bridge to configure the source port in the bus bridge for a transfer. The bus bridge receives an address from the second bus. The bus bridge then stores the address in a register of the source port. The address identifies a destination port on a target peripheral device. The bus bridge then receives data from the first bus and stores the data in a buffer in the bus bridge. The bus bridge transmits one or more address/data pairs to the destination port. The address/data pairs each includes the address and data received from the first bus. The transmitting is performed in response to storing the data in a buffer in the bus bridge. The target peripheral device determines if the buffer in the bus bridge is substantially empty and transmits a flow control command requesting more data in response to determining that the buffer in the bus bridge is substantially empty. A receive port in the bus bridge receives the flow control command requesting more data from the target peripheral device. The bus bridge retrieves data from a memory in the computer system in response to the target peripheral device requesting more data and the receive port in the bus bridge receiving the request for more data from said target peripheral device. The data are stored in the buffer in the bus bridge. The bus bridge transmits one or more address/data pairs to the destination port of said target peripheral device, wherein the address/data pairs each includes the retrieved data.

US005832245A

United States Patent [19]

Gulick

[11] Patent Number: 5,832,245

[45] Date of Patent: Nov. 3, 1998

[54] METHOD FOR ISOCHRONOUS FLOW CONTROL ACROSS AN INTER-CHIP BUS

[75] Inventor: Dale E. Gulick, Austin, Tex.

[73] Assignee: Advanced Micro Devices, Inc.

[21] Appl. No.: 734,295

[22] Filed: Oct. 21, 1996

[51] Int. Cl.[6] G06F 13/37; G06F 13/42

[52] U.S. Cl. 395/309; 395/308; 395/285; 395/876; 395/306

[58] Field of Search 395/284, 285, 395/306-309, 842, 846, 847, 848, 857, 876, 828, 829, 830, 840, 250; 711/147, 150, 152, 154

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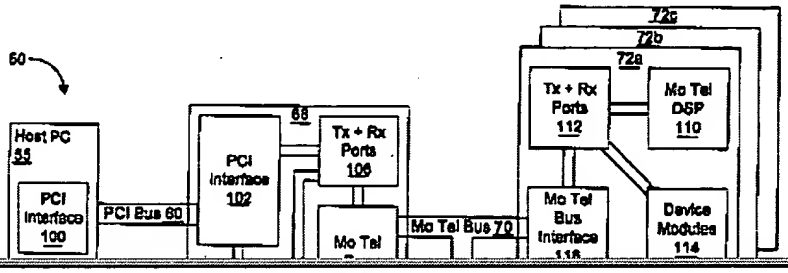
Peripheral Components, Intel, 1995, pp. ix, 1–1 through 1–72.

Primary Examiner—Meng-Ai T. An
Assistant Examiner—Raymond N. Phan
Attorney, Agent, or Firm—Conley, Rose & Tayon

[57] ABSTRACT

A method for communicating data to a plurality of peripheral devices in a computer system, the computer system comprising a first bus, a bus bridge for coupling to the first bus and for interfacing to a second bus, a second bus coupled to the bus bridge, and a plurality of peripheral devices connected to the second bus. The method comprises activating a source port in the bus bridge to configure the source port in the bus bridge for a transfer. The bus bridge receives an address from the second bus. The bus bridge then stores the address in a register of the source port. The address identifies a destination port on a target peripheral device. The bus bridge then receives data from the first bus and stores the data in a buffer in the bus bridge. The bus bridge transmits one or more address/data pairs to the destination port. The address/data pairs each includes the address and data received from the first bus. The transmitting is performed in response to storing the data in a buffer in the bus bridge. The target peripheral device determines if the buffer in the bus bridge is substantially empty and transmits a flow control command requesting more data in response to determining that the buffer in the bus bridge is substantially empty. A receive port in the bus bridge receives the flow control command requesting more data from the target peripheral device. The bus bridge retrieves data from a memory in the computer system in response to the target peripheral device requesting more data and the receive port in the bus bridge receiving the request for more data from said target peripheral device. The data are stored in the buffer in the bus bridge. The bus bridge transmits one or more address/data pairs to the destination port of said target peripheral device, wherein the address/data pairs each includes the retrieved data.

29 Claims, 34 Drawing Sheets



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L5: Entry 1 of 1 File: USPT Jan 20, 2004

DOCUMENT-IDENTIFIER: US 6681274 B2
TITLE: Virtual channel buffer bypass for an I/O node of a computer system

Brief Summary Text (10):
Additionally, there are systems that use a combination of packet-based communications and bus-based communications. For example, a system may connect to a PCI bus and a graphics bus such as AGP. The PCI bus may be connected to a packet bus interface that may then translate PCI bus transactions into packet transactions for transmission on a packet bus. Likewise the graphics bus may be connected to an AGP interface that may translate AGP transactions into packet transactions. Each interface may communicate with a host bridge associated with one of the processors or in some cases to another peripheral device.

Detailed Description Text (3):
Turning now to FIG. 1, a block diagram of one embodiment of a computer system is shown. The computer system includes processors 10A-10D each interconnected by a coherent packet bus 15. Each section of coherent packet bus 15 may form a point-to-point link between each of processors 10A-D. While four processors are shown using point-to point links it is noted that other numbers of processors may be used and other types of buses may interconnect them. The computer system also includes three I/O nodes numbered 20, 30 and 40 each connected together in a chain by I/O packet buses 50B and 50C respectively. I/O packet bus 50A is coupled between host node/processor 10A and I/O node 20. Processor 10A is illustrated as a host node which may include a host bridge for communicating with I/O packet bus 50A. Processors 10B-D may also include host bridges for communication with other I/O packet buses (not shown). The communication links formed by I/O packet bus 50A-C may also be referred to as a point-to-point links. I/O node 20 is connected to a pair of peripheral buses 25A-B. I/O node 30 is connected to a graphics bus 35, while I/O node 40 is connected to an additional peripheral bus 45.

Detailed Description Text (4):
Processors 10A-10D are each illustrative of, for example, an x86 microprocessor such as an Athlon.TM. microprocessor. In addition, one example of a packet bus such as I/O packet bus 50A-50C may be a non-coherent HyperTransport.TM.. Peripheral buses 25A-B and peripheral bus 45 are illustrative of a common peripheral bus such as a peripheral component interconnect (PCI) bus. Graphics bus 35 is illustrative of an accelerated graphics port (AGP), for example. It is understood, however, that other types of microprocessors and other types of peripheral buses may be used.

Detailed Description Text (11):
Referring to FIG. 2, a block diagram of one embodiment of an I/O node is shown. The I/O node is representative of I/O node 20, 30 or 40 of FIG. 1 and will hereafter be referred to as I/O node 20 for simplicity. I/O node 20 of FIG. 2 includes a transaction receiver 110 which is coupled to a transmitter 140 via a command bus 111 and to peripheral interface 150 via a command bus 112. I/O node 20 also includes a transaction receiver 120 which is coupled to a transmitter 130 via a command bus 121 and to peripheral interface 150 via a command bus 122. Peripheral interface 150 is also coupled to transmitters 130 and 140 via a command bus 151 and

to peripheral bus 152. Additionally, I/O node 20 includes a transaction control unit 100 which is coupled to each receiver, each transmitter and to peripheral interface via a control command bus 101. As used herein, a command bus is meant to include signals for command, control and data. Therefore, when a transaction or a command is said to be sent over a respective command bus it is meant to include command and data bits.

Detailed Description Text (16):
Once transaction control unit 100 arbitrates which transaction will be processed, transaction control unit 100 may direct the respective source device to send a pending transaction to the destination device. For example, the transaction control unit 100 selects a control command from its buffer that is representative of a transaction being forwarded from receiver 110 to transmitter 140. Transaction control unit 100 notifies receiver 110 to send the transaction to transmitter 140 via command bus 111. Transmitter 140 may then transmit the transaction to the next node in the chain. The next node may be another I/O node which is either upstream or downstream, or it may be a host node such as host processor 10A of FIG. 1. In addition, transaction control unit 100 and transmitter 140 may include logic (not shown) which indicates to another node whether or not there is free space in the receive buffer.

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L5: Entry 1 of 1 File: USPT Jan 20, 2004

DOCUMENT-IDENTIFIER: US 6681274 B2
TITLE: Virtual channel buffer bypass for an I/O node of a computer system

Brief Summary Text (10):
Additionally, there are systems that use a combination of packet-based communications and bus-based communications. For example, a system may connect to a PCI bus and a graphics bus such as AGP. The PCI bus may be connected to a packet bus interface that may then translate PCI bus transactions into packet transactions for transmission on a packet bus. Likewise the graphics bus may be connected to an AGP interface that may translate AGP transactions into packet transactions. Each interface may communicate with a host bridge associated with one of the processors or in some cases to another peripheral device.

Detailed Description Text (3):
Turning now to FIG. 1, a block diagram of one embodiment of a computer system is shown. The computer system includes processors 10A-10D each interconnected by a coherent packet bus 15. Each section of coherent packet bus 15 may form a point-to-point link between each of processors 10A-D. While four processors are shown using point-to point links it is noted that other numbers of processors may be used and other types of buses may interconnect them. The computer system also includes three I/O nodes numbered 20, 30 and 40 each connected together in a chain by I/O packet buses 50B and 50C respectively. I/O packet bus 50A is coupled between host node/processor 10A and I/O node 20. Processor 10A is illustrated as a host node which may include a host bridge for communicating with I/O packet bus 50A. Processors 10B-D may also include host bridges for communication with other I/O packet buses (not shown). The communication links formed by I/O packet bus 50A-C may also be referred to as a point-to-point links. I/O node 20 is connected to a pair of peripheral buses 25A-B. I/O node 30 is connected to a graphics bus 35, while I/O node 40 is connected to an additional peripheral bus 45.

Detailed Description Text (4):
Processors 10A-10D are each illustrative of, for example, an x86 microprocessor such as an Athlon.TM. microprocessor. In addition, one example of a packet bus such as I/O packet bus 50A-50C may be a non-coherent HyperTransport.TM.. Peripheral buses 25A-B and peripheral bus 45 are illustrative of a common peripheral bus such as a peripheral component interconnect (PCI) bus. Graphics bus 35 is illustrative of an accelerated graphics port (AGP), for example. It is understood, however, that other types of microprocessors and other types of peripheral buses may be used.

Detailed Description Text (11):
Referring to FIG. 2, a block diagram of one embodiment of an I/O node is shown. The I/O node is representative of I/O node 20, 30 or 40 of FIG. 1 and will hereafter be referred to as I/O node 20 for simplicity. I/O node 20 of FIG. 2 includes a transaction receiver 110 which is coupled to a transmitter 140 via a command bus 111 and to peripheral interface 150 via a command bus 112. I/O node 20 also includes a transaction receiver 120 which is coupled to a transmitter 130 via a command bus 121 and to peripheral interface 150 via a command bus 122. Peripheral interface 150 is also coupled to transmitters 130 and 140 via a command bus 151 and

to peripheral bus 152. Additionally, I/O node 20 includes a transaction control unit 100 which is coupled to each receiver, each transmitter and to peripheral interface via a control command bus 101. As used herein, a command bus is meant to include signals for command, control and data. Therefore, when a transaction or a command is said to be sent over a respective command bus it is meant to include command and data bits.

Detailed Description Text (16):
Once transaction control unit 100 arbitrates which transaction will be processed, transaction control unit 100 may direct the respective source device to send a pending transaction to the destination device. For example, the transaction control unit 100 selects a control command from its buffer that is representative of a transaction being forwarded from receiver 110 to transmitter 140. Transaction control unit 100 notifies receiver 110 to send the transaction to transmitter 140 via command bus 111. Transmitter 140 may then transmit the transaction to the next node in the chain. The next node may be another I/O node which is either upstream or downstream, or it may be a host node such as host processor 10A of FIG. 1. In addition, transaction control unit 100 and transmitter 140 may include logic (not shown) which indicates to another node whether or not there is free space in the receive buffer.

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L5: Entry 1 of 1 File: USPT Jan 20, 2004

US-PAT-NO: 6681274
DOCUMENT-IDENTIFIER: US 6681274 B2

TITLE: Virtual channel buffer bypass for an I/O node of a computer system

DATE-ISSUED: January 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ennis; Stephen C.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 978378 [PALM]
DATE FILED: October 15, 2001

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/52; 710/5, 710/7, 710/53, 710/56
US-CL-CURRENT: 710/52; 710/5, 710/53, 710/56, 710/7

FIELD-OF-SEARCH: 710/5, 710/7, 710/52, 710/53, 710/56

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	5809328	September 1998	Nogales et al.	
☐	6278532	August 2001	Heimendinger et al.	
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U.S. patent application serial No. 09/399,281, filed Sep. 17, 1999.

ART-UNIT: 2182

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Farooq; Mohammad O.

ATTY-AGENT-FIRM: Meyertons Hood Kivlin Kowert & Goetzel, P.C. Kivlin; B. Noel

ABSTRACT:

A virtual channel buffer bypass in a computer system input/output node. A control unit of an input/output node for a computer system includes a buffer circuit configured to receive control commands. The buffer circuit may include a plurality of buffers each corresponding to a respective virtual channel of a plurality of virtual channels for storing selected control commands that belong to the respective virtual channel. The buffer circuit may also be configured to determine whether each of the plurality of buffers is empty prior to storing a particular control command corresponding to a given one of the plurality of buffers. In addition, the buffer circuit may be configured to cause the particular control command to bypass the given one of the plurality of buffers in response to determining that each of the plurality of buffers is empty.

14 Claims, 7 Drawing figures

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L4: Entry 13 of 14 File: USPT Mar 21, 2000

DOCUMENT-IDENTIFIER: US 6041016 A
TITLE: Optimizing page size in mixed memory array using address multiplexing

Detailed Description Text (8):
The graphics processor 140 is a high performance graphics controller that perform graphics functions such as 3-D rendering operations, progressive meshes, painting, drawing, etc. The graphics processor 140 is coupled to the host bridge via a graphics bus 145, such as an Accelerated Graphics Port (AGP) bus developed by Intel Corporation. The graphics processor 140 has access to its own graphics local memory 150. The video device 142 provides video input such as digital video disk (DVD), camera, or video cassette recorder (VCR) to the graphics processor 140. The display monitor 144 displays the graphics as generated by the graphics processor 140. The encoder 146 receives the graphics data from the graphics controller 140 and encodes into an analog signal to be compatible for TV display on the TV set 148.

Detailed Description Text (15):
The memory bank address generator 305 generates the bank addresses BA0 and BA1. The memory bank address generator 305 includes N row bank address generators 310.sub.1 to 310.sub.N and a memory bank address multiplexer 320. Each of the row bank address generators 310.sub.1 to 310.sub.N receives the control data from the memory controller 250 (FIG. 2) via the command bus, and the row addresses RA11 to RA14 from the memory controller 250 via the row address bus. The row bank address generators 310.sub.1 to 310.sub.N generate the row bank addresses R1BA0, R1BA1, to RNBA0, RNBA1, respectively. The memory bank address multiplexer receives the row bank addresses R1BA0, R1BA1 to RNBA0, RNBA1 and generates the memory bank addresses BA0 and BA1.

Detailed Description Text (16):
The memory address generator 330 receives the control data from the memory controller 250 (FIG. 2) via the command bus and the row addresses RA0 to RA26 via the row address bus. The memory address generator 330 generates the memory addresses A0 to A11.

Detailed Description Text (27):
The row J configuration register 410.sub.J stores the configuration data as written by the memory controller or the host processor during initialization via the command bus. The configuration data include the size, or organization, and the page size of the memory devices used in the corresponding row. In one embodiment, the row J configuration register 410.sub.J includes five bits: three bits (RJS[2:0]) for the memory size and two bits (RJPS[1:0]) for page size. In this configuration, the memory array can accommodate eight different memory sizes and four different page sizes. Of course, more memory and page sizes can be accommodated using more bits in the configuration register.

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L7: Entry 12 of 12 File: USPT May 27, 2003

US-PAT-NO: 6571321
DOCUMENT-IDENTIFIER: US 6571321 B2

TITLE: Read exclusive for fast, simple invalidate

DATE-ISSUED: May 27, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rowlands; Joseph B.	Santa Clara	CA		
Carlson; Michael D.	Mountain View	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Broadcom Corporation	Irvine	CA			02

APPL-NO: 09/ 917432 [PALM]
DATE FILED: July 27, 2001

INT-CL: [07] G06 F 12/00

US-CL-ISSUED: 711/141; 711/146
US-CL-CURRENT: 711/141; 711/146

FIELD-OF-SEARCH: 711/141, 711/146, 711/147

PRIOR-ART-DISCLOSED:

OTHER PUBLICATIONS

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ART-UNIT: 2188

PRIMARY-EXAMINER: Verbrugge; Kevin

ATTY-AGENT-FIRM: Merkel; Lawrence J. Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C.

ABSTRACT:

An agent, in response to a write to a shared block, is configured to initiate a read exclusive transaction on an interface on which the agent communicates. Additionally, the agent is configured to indicate, to a responding agent or agents on the interface, that a data transfer is not required from the responding agent or agents in response to the read exclusive transaction. In one embodiment, the agent indicates to the responding agents that a data transfer is not required in a response phase of the transaction. Specifically, the agent may respond in such a way that the agent indicates that it will provide the data (i.e. that the agent will provide the data to itself). For example, the agent may respond with an exclusive ownership indication. On the interface for such an embodiment, an exclusive ownership response may require that the agent having exclusive access respond with the data.

24 Claims, 7 Drawing figures

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L7: Entry 12 of 12 File: USPT May 27, 2003

DOCUMENT-IDENTIFIER: US 6571321 B2
TITLE: Read exclusive for fast, simple invalidate

Detailed Description Text (10):
I/O bridges 20A-20B link one or more I/O interfaces (e.g. I/O interfaces 22A-22B for I/O bridge 20A and I/O interfaces 22C-22D for I/O bridge 20B) to bus 24. I/O bridges 20A-20B may serve to reduce the electrical loading on bus 24 if more than one I/O interface 22A-22B is bridged by that I/O bridge. Generally, I/O bridge 20A performs transactions on bus 24 on behalf of I/O interfaces 22A-22B and relays transactions targeted at an I/O interface 22A-22B from bus 24 to that I/O interface 22A-22B. Similarly, I/O bridge 20B generally performs transactions on bus 24 on behalf of I/O interfaces 22C-22D and relays transactions targeted at an I/O interface 22C-22D from bus 24 to that I/O interface 22C-22D. In one implementation, I/O bridge 20A may be a bridge to a PCI interface (e.g. I/O interface 22A) and to a Lightning Data Transport (LDT) I/O fabric (also known as HyperTransport) developed by Advanced Micro Devices, Inc. (e.g. I/O interface 22B). Other I/O interfaces may be bridged by I/O bridge 20B. Other implementations may bridge any combination of I/O interfaces using any combination of I/O bridges. I/O interfaces 22A-22D may include one or more serial interfaces, Personal Computer Memory Card International Association (PCMCIA) interfaces, Ethernet interfaces (e.g. media access control level interfaces), Peripheral Component Interconnect (PCI) interfaces, LDT interfaces, etc.

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L9: Entry 2 of 5 File: USPT Feb 10, 2004

DOCUMENT-IDENTIFIER: US 6691185 B2
TITLE: Apparatus for merging a plurality of data streams into a single data stream

Brief Summary Text (4):
In an effort to increase I/O bandwidth in high performance processor based systems, a number of companies have developed the HyperTransport ("HT") I/O interconnect structure. Briefly, the HT I/O bus structure is a scalable device level architecture that provides a significant increase in transaction throughput over existing I/O bus architectures such as Peripheral Component Interconnect ("PCI") and Advanced Graphics Port ("AGP").

Other Reference Publication (3):
API NetWorks, Inc., HyperTransport: Universal Interconnect Solution for I/O, Mar. 7, 2001.

Other Reference Publication (5):
API NetWorks, Inc., HyperTransport Applications in Embedded DSP/RISC Based Systems: A High-Bandwidth, Low-Complexity Embedded I/O Interconnect Architecture.

CLAIMS:

2. The I/O device of claim 1 wherein the I/O device is a HyperTransport I/O device.

3. The I/O device of claim 1, wherein the input port is coupled to a HyperTransport I/O device by a link.

11. The I/O device of claim 1, wherein the output port is coupled to a HyperTransport I/O device by a link.

13. The I/O device of claim 12 wherein the I/O device is a HyperTransport I/O device.

14. The I/O device of claim 12, wherein the first input port is coupled to a first HyperTransport I/O device by a first link and the second input port ID is coupled to a second HyperTransport I/O device by a second link.

22. The I/O device of claim 12, wherein the output port is coupled to a HyperTransport I/O device by a link.

24. The I/O device of claim 23 wherein the I/O device is a HyperTransport I/O device.

25. The I/O device of claim 23, wherein the first internal port is coupled to a first HyperTransport I/O device by a first link and the second internal port ID is coupled to a second HyperTransport I/O device by a second link.

33. The I/O device of claim 23, wherein the output port is coupled to a HyperTransport I/O device by a link.

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L9: Entry 2 of 5 File: USPT Feb 10, 2004

US-PAT-NO: 6691185
DOCUMENT-IDENTIFIER: US 6691185 B2

TITLE: Apparatus for merging a plurality of data streams into a single data stream

DATE-ISSUED: February 10, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Avery; James M.	Westford	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Sun Microsystems, Inc.	Palo Alto	CA			02

APPL-NO: 09/ 905281 [PALM]
DATE FILED: July 13, 2001

PARENT-CASE:
This patent application discloses subject matter that is related to the subject matter disclosed in U.S. patent application Ser. No. 09/905,483, entitled "Method for Merging a Plurality of Data Streams into a Single Data Stream" filed on even date herein. The above Patent Application is hereby incorporated by reference.

INT-CL: [07] G06 F 13/00

US-CL-ISSUED: 710/52; 710/62, 710/72, 370/389, 370/423, 370/412
US-CL-CURRENT: 710/52; 370/389, 370/412, 370/423, 710/62, 710/72

FIELD-OF-SEARCH: 370/351-396, 370/412, 370/422-423, 709/234, 709/238, 710/11, 710/29-35, 710/52-57, 710/62, 710/67

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

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☐	4860357	August 1989	Avery	381/41
☐	4926418	May 1990	Cidon	370/85.5
☐	5245609	September 1993	Ofek	370/94.3

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☐	5687325	November 1997	Chang	710/104
☐	5889776	March 1999	Liang	370/389
☐	6058436	May 2000	Kosco	710/11
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Edward Ott, Chaos in Dynamical Systems, 1993.

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ART-UNIT: 2182

PRIMARY-EXAMINER: Shin; Christopher B.

ATTY-AGENT-FIRM: Park, Vaughan & Fleming LLP

ABSTRACT:

An I/O device that includes: an input port; an input buffer coupled to the input port; an internal port operable to store packets generated by the I/O device; an internal buffer coupled to the internal port; a plurality of packet ID arrival registers coupled to the input port and the internal port; autocorrelation logic coupled to the plurality of packet ID arrival registers; an arbiter coupled to the autocorrelation logic; a packet selector coupled to the arbiter, the input buffer and the internal buffer; and an output port coupled to the packet selector.

36 Claims, 12 Drawing figures